IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1-20 (Cancelled)

21. (Currently Amended) A method of manufacturing a semiconductor device having a MOSFET and an MODEET on a single semiconductor substrate, comprising:

forming, on the semiconductor substrate, a single-crystal silicon including a device isolation insulation film;

covering the semiconductor substrate in a MOSFET forming region with the device isolation insulation film;

forming a groove in which the device isolation insulation film is exposed, and the single-crystal silicon is exposed, in a MODFET forming region;

forming, in the groove, an intrinsic region for the MODFET in the groove using selective growth; at least substantially removing the device isolation insulation film;

forming a gate insulation film and a gate electrode for the MOSFET; and

forming a gate insulation film and a gate electrode for the MODFET.

22. (Original) The method of claim 21, further comprising:
forming a silicon nitride film on a lateral surface of the groove.

23. (Original) The method of claim 21, further comprising:

selective growth of a buffer layer comprising a single-crystal silicon-germanium on a single-crystal silicon;

wherein the MODFET is a P-type, and wherein said forming, in the groove, an intrinsic region for the MODFET comprises:

selective growth of a carrier supply layer comprising a single-crystal silicon-germanium doped with a P-type dopant, a spacer layer comprising a single-crystal silicon germanium, a channel layer comprising a single-crystal silicon-germanium, and a cap layer comprising a single-crystal silicon, successively on the buffer layer.

24. (Original) The method of claim 23, wherein the germanium content of the channel layer is higher than the germanium content of the spacer layer.

25. (Original) The method of claim 21, wherein the MODFET is a P-type, further comprising:

selective growth of a buffer layer comprising a single-crystal silicon-germanium on a single-crystal silicon;

wherein said forming, in the groove, an intrinsic region for the MODFET comprises: selective growth of a first spacer layer comprising a single-crystal silicon-germanium, a channel layer comprising a single-crystal silicon-germanium, a second spacer layer comprising a single-crystal silicon-germanium, a carrier supply layer comprising a single-crystal silicon-germanium doped with a P-type dopant, and a cap layer comprising a single-crystal silicon, successively on the buffer layer.

26. (Original) The method of claim 25, wherein the germanium content of the channel layer is higher than the germanium content of the first spacer layer.

27. (Original) The method of claim 21, wherein the MODFET is an N-type, further comprising:

selective growth of a buffer layer comprising a single-crystal silicon-germamium on a single-crystal silicon;

wherein said forming, in the groove, an intrinsic region for the MODFET comprises:

selective growth of a first spacer layer comprising a single-crystal silicon-germanium, a channel layer comprising a single-crystal silicon, a second spacer layer comprising a single-crystal silicon-germanium, and a cap layer comprising a single crystal silicon, successively on the buffer layer single-crystal silicon.

28. (Original) The method of claim 21, wherein the MODFET is an P-type, further comprising:

selective growth of a buffer layer comprising a single-crystal silicon-germanium on a single-crystal silicon;

wherein said forming, in the groove, an intrinsic region for the MODFET comprises:

selective growth of a carrier supply layer comprising a single-crystal silicon-germanium doped with an N-type dopant, a first spacer layer comprising a single-crystal silicon-germanium, a channel layer comprising a single-crystal silicon containing no dopant, a second spacer layer comprising a single-crystal silicon-germanium, and a cap layer comprising a single-crystal silicon, successively on the buffer layer single-crystal silicon.

29. (Original) The method of claim 21, wherein said forming, in the groove, an intrinsic region for the MODFET comprises conducting a CVD including a halogenous gas.

30. (Original) The method of claim 29, wherein a source gas for silicon comprises at least one selected from the group consisting of silicon hydride and chloride, and wherein a source gas for germanium comprises at least one selected from the group consisting of germanium hydride and chloride, and wherein the halogenous gas comprises a hydrogen chloride gas of flow rate in a range of about 20 to about 80 ml/min.

31. (Original) The method of claim 21, wherein said forming, in the groove, an intrinsic region for the MODFET comprises conducting a gas source MBE including a halogenous gas.

32. (Original) The method of claim 31, wherein disilane is a source gas for silicon, and wherein germane is a source gas for germanium, and wherein a hydrogen chloride gas is the halogenous gas, and wherein the flow rate of the hydrogen chloride gas is in a range of about 5 to about 10 ml/min.

33-51 (Cancelled)

Please enter the following amendments and remarks:

STATUS OF THE CLAIMS

Claims 21-32 are pending in the Application.

Claims 21-32 have been objected to by the Examiner.

Claim 21 has been amended herein.

Reconsideration of the present Application is respectfully requested.